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EXAMINER	
STIGLIC, RYAN M	

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2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/556,450	NG ET AL.	
	Examiner	Art Unit	
	RYAN M. STIGLIC	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are pending and have been examined.

2. Claims 1-23 are rejected.

Claim Objections

3. Claim 21 is objected to because of the following informalities: Claim 21 recites in part "the host controller is further configured to respond to memory transactions scheduled by the host controller". It is assumed the second recitation of host controller was a typographical error and the term "host microprocessor" was intended such that the claims are consistent with the teachings of the originally filed specification at page 4, lines 23-25. Appropriate correction is required.

Response to Arguments

4. Applicant's arguments filed April 20, 2009 have been fully considered but they are not persuasive.

In regards to applicant's arguments that Wang does not disclose an "internal memory having a plurality of locations mapped in the host microprocessor" (*page 9 of the remarks*) the Examiner respectfully disagrees. Figure 6 of Wang shows the internal memory of the USB Host Controller mapped into data memory, control registers, etc. The memory supports address in the range of 000h to FFFh. This 12 bit address directly correlates to the 12 bit address bus of the μP interface

104. As such, the internal memory of the Host Controller is shown to be mapped the μP since the μP is able to directly access portions of the internal memory through the use of the μP interface and the 12-bit address.

Furthermore, Wang recites (***emphasis added***):

> [0138] The host controller system 100 does not have a bus mastering ability as in a PCI bus in the Universal Host Controller Interface (UHCI) or the Open Host Controller Interface (OHCI). However, the USB host stack (i.e., USB Driver and Host Controller Driver) in many operating systems is designed to operate with a host controller system that does have bus mastering capabilities. For example, using UHCI or OHCI interfaces, data can be moved between the system memories in response to signals from the host controller as the system bus can be slaved to the host controller. As discussed above, however, with embedded systems, the system bus is only under the control of the host microprocessor. Hence, such host stack are often not able to be used with such embedded USB systems.
>
> [0140] More specifically, in one embodiment shown in FIG. 9a, the USB Engine 168 makes use of the interrupt from the host controller system 100 to activate an interrupt handler routine which pushes transaction descriptors 110 and data from the microprocessor 102 system memory to the host controller system 100 memory and pulls transaction status and data from the host controller system 100 memory to the microprocessor 102 system memory. ***This invention is able to provide an OHCI or UHCI interface to the HCD without requiring bus mastering ability as in a PCI bus controller.*** Using this invention, USB host stack that is written for an operating system and OHCI or UHCI type of host controllers requiring bus mastering may be interfaced directly with the embedded host controller system 100 which does not have bus mastering. ***The host controller system 100 will appear as an OHCI or UHCI to an operating system that has OHCI or UHCI USB host support*** such as Windows CE. In essence, the USB Engine 168 makes use of the interrupt from the host controller system 100 to activate an interrupt handler routine to handle the bidirectional communication between the microprocessor memory and the host controller system 100 to accomplish the same objective in a bus mastering bus.

Thus the microprocessor runs the USB host stack to interface with the host controller 100.

Regarding the OHCI interface, paragraph [0141] of Wang recites (***emphasis added***):

> ***In OHCI, there is a segment in shared main memory, called Host Controller Communications Area (HCCA), established by the HCD and is used for communication between the HCD and the host controller system 100***. There are two communication channels between the host controller system 100 and the HCD. The first channel uses the registers located in the host controller system 100. ***It may also use a segment of the microprocessor 102 memory to control the functions of the host controller system 100***. The USB Engine 168 shown in FIG. 9a makes use of the interrupt from the host controller system 100 to activate an interrupt handler routine to handle this communication channel by pushing data to the control registers of the host controller system 100 and the said segment of the microprocessor 102 memory. The USB Engine 168 also maintains a pointer to the HCCA in the system memory. The HCCA is the second communication channel. The USB Engine 168 makes use of the interrupt from the host controller system 100 to activate an interrupt handler routine to handle this channel which may be bidirectional. The HCCA contains the head pointers to the interrupt Endpoint Descriptor lists, the head pointer to the done queue, and status information associated with start-of-frame processing.

Therefore, in addition to the internal memory of the Host Controller being mapped for microprocessor access, the host controller system and thus the internal memory of the host controller are memory-mapped to a segment of microprocessor's memory (e.g. system memory) such that portions of the Host Controller (e.g. internal memory) are accessed when the host microprocessor addressed the mapped addresses of the system memory (As per paragraphs 0138, 0140 and 0141 of Wang).

Applicant's argument that Hamdi fails to cure the deficiencies of Wang is not persuasive for the reasons above.

In regards to applicant's arguments that the combination of Wang in view of Hamdi would render the Host Controller inoperative the Examiner respectfully disagrees (*page 10 of the remarks*). Applicant contends that absent a collision avoidance procedure (LOOK UP HIS EXACT ARGUMENT) the proposed combination of Wang and Hamdi would be inoperative. The combination of Wang and Hamdi suggests moving the memory of Wang [*Fig. 1A, 32*] onto the µP/memory bus. Insofar as the Host Controller of Wang is configured to operate only as a slave device on the µP/memory bus, as is the system memory, the only master device on the µP/memory bus would be the µP. As such, there would be master device contention and thus the combination of Wang and Hamdi would not be inoperative for the reasons proposed by the applicant.

Applicant's arguments regarding claims 10 and 23 recite similar arguments to those presented with respect to claim 1 above and are therefore not persuasive for the reasons above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2002/0116565 (hereinafter Wang) in view of US Patent No. 6,912,651 (hereinafter Hamdi).

References made below to paragraphs [xxxx] are intended to refer to relevant portions of Wang. References made below to column and line numbers [col. x, line y] are intended to refer to relevant portions of Hamdi. References to Figures [Fig. X, item y] are intended to refer to relevant figures of Wang unless otherwise noted.

As previously discussed in the Final Office Action dated January 18, 2008, Wang discloses: a host controller (Fig. 1A, 100), for use in a bus communication device comprising a host microprocessor and a system memory, the host controller comprising: a first interface (Fig. 1A, the left side of host controller 100) for connection to a memory bus (Fig. 1A, 31) which connects the host microprocessor (Fig. 1A, 24) and the system memory (Fig. 1A, 32), such that the host controller is adapted to act only as a slave on the memory bus ([0138-0140] describe how the host controller is not required to act as a bus master); an internal memory (Fig. 1A, 30), for storing a plurality of transfer-based transfer descriptors received through the first interface ([0041]); and a second interface (Fig. 1A, 28 the right side of host controller), for connection to an external bus (Fig. 1A, the lines connecting to USB devices 26), wherein the host controller is adapted to: execute stored transfer-based transfer descriptors ([0041-0042]); update the content of the stored transfer-based transfer descriptors on execution ([0051] "…and updates, in state 76, a record in the transaction descriptor…"); and copy the updated stored transfer-based transfer

descriptors to the system memory ([0138-0140] describes the processes of where the host controller transfers data to the system memory under the control of the microprocessor). While the host controller provides a connection to system memory and a microprocessor, Wang does not expressly disclose providing a direct connection to both system memory and the microprocessor.

Hamdi teaches (Fig. 6) a computer system having USB Host Controller **608** that is directly connected to a system/memory bus **604** which directly interfaces system memory **606** and processor **602** (col. 11, ll. 42-64). By directly interconnecting the USB Host Controller, system memory and processor via a common bus, the USB Host Controller access the system memory directly and is not burdened with additional latency associated with having to access the system memory through a processor.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to directly connect the USB Host Controller of Wang to the system memory and microprocessor as suggested by Hamdi such that memory access latency is reduced because the USB Host Controller does not need to access the system memory through the microprocessor.

For claim 1 Wang in view of Hamdi teach:

A host controller (Fig. 1A, 100), for use in a bus communication device comprising a host microprocessor and a system memory, the host controller comprising:

- a first interface (Fig. 1A, the left side of host controller 100) for direct connection (Hamdi teaches, Fig. 6, providing a direct connection between the host controller, microprocessor and system memory [col. 11, ll. 42-64].) to a memory bus (Fig. 1A, 31) which connects the host microprocessor (Fig. 1A, 24) and the system memory (Fig. 1A, 32), such that the host controller is adapted to act only as a slave on the memory bus ([0138-0140] describe how the host controller is not required to act as a bus master);
- an internal memory (Fig. 1A, 30), for storing a plurality of transfer-based transfer descriptors received through the first interface ([0041]), said internal memory having a plurality of locations mapped in the host microprocessor (Figure 6 of Wang shows the internal memory of the USB Host Controller mapped into data memory, control registers, etc. The memory supports address in the range of 000h to FFFh. This 12 bit address directly correlates to the 12 bit address bus of the µP interface 104. As such, the internal memory of the Host Controller is shown to be mapped the µP since the µP is able to directly access portions of the internal memory through the use of the µP interface and the 12-bit address. In addition to the internal memory of the Host Controller being mapped for microprocessor access, the host controller system and thus the internal memory of the host controller are memory-mapped to a segment of microprocessor's memory (e.g. system memory) such that portions of the Host Controller (e.g. internal memory) are accessed when the host microprocessor addressed the mapped addresses of the system memory (As per paragraphs 0138, 0140 and 0141 of Wang).); and
- a second interface (Fig. 1A, 28 the right side of host controller), for connection to an external bus (Fig. 1A, the lines connecting to USB devices 26),

- wherein the host controller is adapted to:
    - execute stored transfer-based transfer descriptors ([0041-0042]);
    - update the content of the stored transfer-based transfer descriptors on execution ([0051] "…and updates, in state 76, a record in the transaction descriptor…"); and
    - copy the updated stored transfer-based transfer descriptors to the system memory ([0138-0140] describes the processes of where the host controller transfers data to the system memory under the control of the microprocessor.).

For claim 2 Wang in view of Hamdi teach:

A host controller as claimed in claim 1, wherein the internal memory is a dual-port RAM ([0054]).

For claim 3 Wang in view of Hamdi teach:

A host controller as claimed in claim 1, wherein the internal memory is a single-port RAM, and the host controller further comprises an arbiter to allow data to be written to and read from the RAM essentially simultaneously ([0056] "The batch memory 30 is preferably organized as to be able to receive USB transactions from the host microprocessor 24 for one batch while the host controller system 100 is acting on another batch.").

For claim 4 Wang in view of Hamdi teach:

A host controller as claimed in claim 1, wherein the internal memory is divided into two parts (Fig. 5, first part 106 and second part 116), and is adapted to store transfer-based transfer

descriptor headers in a first part ([0060]), and to store transfer-based transfer descriptor payload data in a second part ([0063]).

For claim 5 Wang in view of Hamdi teach:

A host controller as claimed in claim 4, wherein the first part of the internal memory is sub-divided into two sub-parts, and is adapted to store transfer descriptor headers relating to periodic transfers in a first sub-part ([0062,0065] "isochronous transaction"), and to store transfer descriptor headers relating to asynchronous transfers in a second sub-part ([0065] "bulk transaction"]).

For claim 6 Wang in view of Hamdi teach:

A host controller as claimed in claim 5, wherein the host controller is adapted to scan the first sub-part of the internal memory once in each micro-frame ([0065] "For example, five transactions can be scheduled for a total of 1,280 bytes in one ms: one isochronous of 1023 and four bulk or interrupt transactions of 64 bytes each." The host controller therefore scanned the control memory [CM] once in the micro-frame thus meeting the claim limitation.), and is adapted to scan the second sub-part continuously throughout each micro-frame ([0065] "For example, five transactions can be scheduled for a total of 1,280 bytes in one ms: one isochronous of 1023 and four bulk or interrupt transactions of 64 bytes each." The host controller therefore scanned the control memory [CM] throughout the micro-frame thus meeting the claim limitation.).

For claims 7 and 11 Wang in view of Hamdi teach:

A host controller as claimed in claim 1, wherein the host controller is a USB host controller and the second interface is a USB bus interface (Fig. 1A, [0003, 0016]).

For claims 8 and 12 Wang in view of Hamdi teach:

A host controller as claimed in claim 1, wherein the internal memory is adapted to store multiple micro-frames of transfer descriptors ([0056] "The batch memory 30 is preferably organized so as to be able to receive USB transactions from the host microprocessor 24 for one batch while the host controller system 100 is acting on another batch."), and to execute the stored transfer descriptors without intervention from the host microprocessor ([0042] describes how the host controller executes the stored transfer descriptors without the microprocessor.).

For claim 9 Wang in view of Hamdi teach:

A host controller as claimed in claim 8, wherein each of the multiple micro-frames of transfer descriptors may store payload data relating to one or more of isochronous, interrupt and bulk data transfers ([0063, 0070] describe a data memory 116 [Fig. 5] holds data for USB transactions of type isochronous, bulk or interrupt [0062,0065].).

For claim 10 Wang in view of Hamdi teach:

A bus communication device, comprising:

- a host microprocessor (Fig. 1A, 24);
- a system memory (Fig. 1A, 32);

- a memory bus, which connects the host microprocessor and the system memory (Fig. 1A line connecting 24 and 32; and
- a host controller (Fig. 1A, 100), wherein the host microprocessor is adapted to form transfer-based transfer descriptors, and write the transfer-based transfer descriptors to the system memory and to the host controller, and wherein the host controller comprises:
    - a first interface (Fig. 1A, the left side of host controller 100) for direct connection (Hamdi teaches, Fig. 6, providing a direct connection between the host controller, microprocessor and system memory [col. 11, ll. 42-64].) to a memory bus (Fig. 1A, 31) which connects the host microprocessor (Fig. 1A, 24) and the system memory (Fig. 1A, 32), such that the host controller is adapted to act only as a slave on the memory bus ([0138-0140] describe how the host controller is not required to act as a bus master);
    - an internal memory (Fig. 1A, 30), for storing a plurality of transfer-based transfer descriptors received through the first interface ([0041]), said internal memory having a plurality of locations mapped in the host microprocessor (Figure 6 of Wang shows the internal memory of the USB Host Controller mapped into data memory, control registers, etc. The memory supports address in the range of 000h to FFFh. This 12 bit address directly correlates to the 12 bit address bus of the μP interface 104. As such, the internal memory of the Host Controller is shown to be mapped the μP since the μP is able to directly access portions of the internal memory through the use of the μP interface and the 12-bit address. In addition to the internal memory of the Host Controller being mapped for

microprocessor access, the host controller system and thus the internal memory of the host controller are memory-mapped to a segment of microprocessor's memory (e.g. system memory) such that portions of the Host Controller (e.g. internal memory) are accessed when the host microprocessor addressed the mapped addresses of the system memory (As per paragraphs 0138, 0140 and 0141 of Wang).); and

- a second interface (Fig. 1A, 28 the right side of host controller), for connection to an external bus (Fig. 1A, the lines connecting to USB devices 26),
- wherein the host controller is adapted to:
  - execute stored transfer-based transfer descriptors ([0041-0042]);
  - update the content of the stored transfer-based transfer descriptors on execution ([0051] "…and updates, in state 76, a record in the transaction descriptor…"); and
  - copy the updated stored transfer-based transfer descriptors to the system memory ([0138-0140] describes the processes of where the host controller transfers data to the system memory under the control of the microprocessor).

For claims 13 and 18 Wang in view of Hamdi teach:

(new) A host controller as claimed in claim 1, wherein the first interface comprises:

a memory mapped input/output (Fig. 5, 116; The data from the input/output data from the transfer descriptors is memory mapped to memory at addresses 800h to FFFh.); a memory

management unit (Fig. 5, 104 manages access to memory 106/110/116.); and a slave direct memory access (DMA) controller (Fig. 5, 104 provides direct memory access to memory 106/110/116.).

For claim 14 Wang in view of Hamdi teach:

A host controller as claimed in claim 1, wherein the first interface comprises registers (Wang discloses a plurality of registers in paragraphs 0071-0099.).

For claims 17 and 20 Wang in view of Hamdi teach:

A host controller as claimed in claim 1, further comprising an external connection to the first interface, wherein the external connection is configured to carry control and interrupt signals (Fig. 1A shows an external bus configured to carry control signals and an interrupt signal from the host controller to the host microprocessor.).

For claims 15, 16 and 19 Wang in view of Hamdi teach:

A bus communication device as claimed in claim 18, wherein the host controller further comprises:

a logic unit, wherein the logic unit comprises the second interface (Fig. 5, 120/130); and

an internal bus coupled between the registers and the logic unit, wherein the internal bus is configured to carry control signals from the registers to the logic unit (Any of the internal buses of the host controller are configured to carry control and data signals from the registers to the

logic unit because the registers store command bits (e.g. resets) or status (e.g. a transfer is complete).).

For claim 21 Wang in view of Hamdi teach:

The host controller as claimed in claim 1 wherein the host controller is further configured to respond to memory transactions scheduled by the host controller (Figure 6 of Wang shows the internal memory of the USB Host Controller mapped into data memory, control registers, etc. The memory supports address in the range of 000h to FFFh. This 12 bit address directly correlates to the 12 bit address bus of the μP interface 104. As such, the internal memory of the Host Controller is shown to be mapped the μP since the μP is able to directly access portions of the internal memory through the use of the μP interface and the 12-bit address. In addition to the internal memory of the Host Controller being mapped for microprocessor access, the host controller system and thus the internal memory of the host controller are memory-mapped to a segment of microprocessor's memory (e.g. system memory) such that portions of the Host Controller (e.g. internal memory) are accessed when the host microprocessor addressed the mapped addresses of the system memory (As per paragraphs 0138, 0140 and 0141 of Wang). Thus the host controller is configured to respond to memory transactions scheduled by the host microprocessor.).

For claim 22 Wang in view of Hamdi teach:

The bus communication device as claimed in claim 10, wherein the plurality of locations of the internal memory mapped to the system memory are configured for access by the host

microprocessor when the host microprocessor addresses the mapped addresses of the system memory (Figure 6 of Wang shows the internal memory of the USB Host Controller mapped into data memory, control registers, etc. The memory supports address in the range of 000h to FFFh. This 12 bit address directly correlates to the 12 bit address bus of the μP interface 104. As such, the internal memory of the Host Controller is shown to be mapped the μP since the μP is able to directly access portions of the internal memory through the use of the μP interface and the 12-bit address. In addition to the internal memory of the Host Controller being mapped for microprocessor access, the host controller system and thus the internal memory of the host controller are memory-mapped to a segment of microprocessor's memory (e.g. system memory) such that portions of the Host Controller (e.g. internal memory) are accessed when the host microprocessor addressed the mapped addresses of the system memory (As per paragraphs 0138, 0140 and 0141 of Wang).).

For claim 23 Wang in view of Hamdi teach:

A method of executing bus transactions with a host controller

comprising:

- configuring the host controller as a slave ([0138-0140] describe how the host controller is not required to act as a bus master and thus acts only as a slave) on a memory bus (Fig. 1A, 31), the memory bus directly connected (Hamdi teaches, Fig. 6, providing a direct connection between the host controller, microprocessor and system memory [col. 11, ll. 42-64].) to the host controller (Fig. 1A, 100), a host microprocessor (Fig. 1A, 24), and a system memory (Fig. 1A, 32);

- configuring address space of an internal memory (Fig. 1A, 30) to be mappable in the host processor, said address space accessible via the memory bus (Figure 6 of Wang shows the internal memory of the USB Host Controller mapped into data memory, control registers, etc. The memory supports address in the range of 000h to FFFh. This 12 bit address directly correlates to the 12 bit address bus of the μP interface 104. As such, the internal memory of the Host Controller is shown to be mapped the μP since the μP is able to directly access portions of the internal memory through the use of the μP interface and the 12-bit address. In addition to the internal memory of the Host Controller being mapped for microprocessor access, the host controller system and thus the internal memory of the host controller are memory-mapped to a segment of microprocessor's memory (e.g. system memory) such that portions of the Host Controller (e.g. internal memory) are accessed when the host microprocessor addressed the mapped addresses of the system memory (As per paragraphs 0138, 0140 and 0141 of Wang).);
- configuring the internal memory to store a plurality of transfer-based transfer descriptors received via the memory bus (See at least paragraph [0041].);
- reading transfer-based transfer descriptors from the internal memory (See at least paragraphs [0041-0042].);
- executing the transfer-based transfer descriptors (See at least paragraphs [0041-0042].); and
- updating the content of the transfer-based transfer descriptors on execution ([0051] "…and updates, in state 76, a record in the transaction descriptor…").

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RYAN M. STIGLIC whose telephone number is (571)272-3641. The examiner can normally be reached on Monday - Friday (7:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571.272.3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ryan M Stiglic/
Examiner, Art Unit 2111